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UNITED STATES DISTRICT COURT  
 NORTHERN DISTRICT OF CALIFORNIA  
 SAN JOSE DIVISION

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 15 HTC CORPORATION and HTC  
 16 AMERICA, INC.,

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 18 Plaintiffs,

19 v.  
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20 TECHNOLOGY PROPERTIES  
 21 LIMITED, PATRIOT SCIENTIFIC  
 22 CORPORATION and ALLIACENSE  
 23 LIMITED,  
 24 Defendants.

25 Case No. C 08 00882 JF  
 26 (related to C 08 00877 JF and C 08 00884)

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1 I, Mark F. Lambert, declare:

2 1. I am an attorney with the law firm of White & Case LLP, counsel of record in this  
3 action for plaintiffs HTC Corporation (“HTC”) and HTC America (“HTC America”). I am  
4 admitted to practice before this Court. I have personal knowledge of the facts contained within  
5 this declaration and, if called as a witness, would and could testify competently thereto.

6 2. Attached hereto as Exhibit A are face pages for United States Patent Numbers  
7 5,809,336 (“336 patent”); 5,784,584 (“584 patent”); 5,440,749 (“749 patent”); 6,598,148  
8 (“148 patent”) and/or 5,530,890 (the “890 Patent”) (collectively the “patents-in-suit”).

9 I declare under penalty of perjury that the foregoing is true and correct. Executed in Palo  
10 Alto, California on July 11, 2008

11 Dated: July 11, 2008

WHITE & CASE LLP

13 By: /s/ Mark F. Lambert

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# EXHIBIT A



US005809336A

**United States Patent** [19]  
**Moore et al.**

[11] **Patent Number:** **5,809,336**  
[45] **Date of Patent:** **Sep. 15, 1998**

[54] **HIGH PERFORMANCE MICROPROCESSOR HAVING VARIABLE SPEED SYSTEM CLOCK**

[75] Inventors: **Charles H. Moore**, Woodside; **Russell H. Fish, III**, Mt. View, both of Calif.

[73] Assignee: **Patriot Scientific Corporation**, San Diego, Calif.

[21] Appl. No.: **484,918**

[22] Filed: **Jun. 7, 1995**

**Related U.S. Application Data**

[62] Division of Ser. No. 389,334, Aug. 3, 1989, Pat. No. 5,440,749.

[51] **Int. Cl.<sup>6</sup>** ..... **G06F 1/04**

[52] **U.S. Cl.** ..... **395/845**

[58] **Field of Search** ..... 395/500, 551,  
395/555, 845

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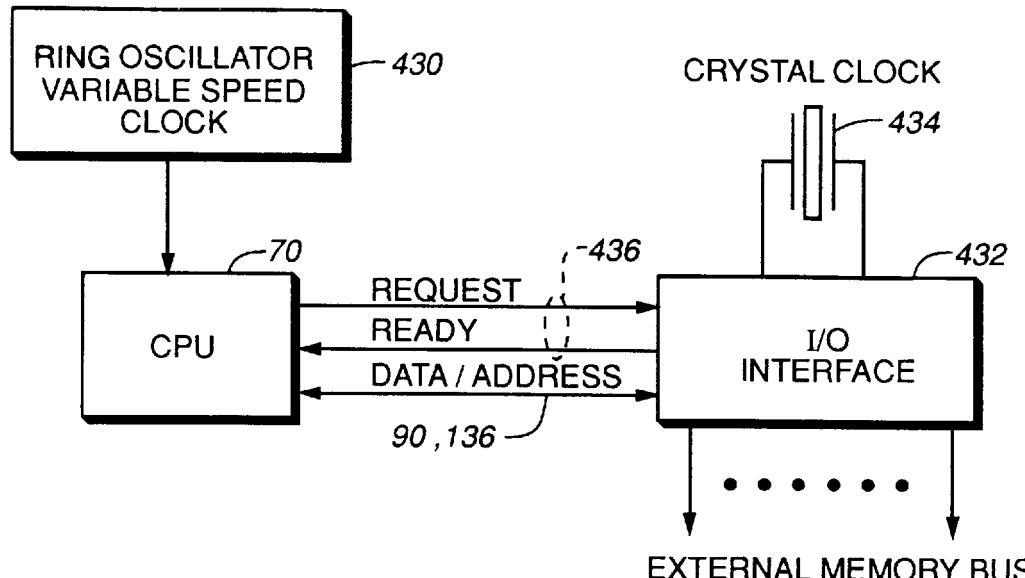
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*Primary Examiner—David Y. Eng  
Attorney, Agent, or Firm—Cooley Godward LLP*

[57] **ABSTRACT**

A high performance, low cost microprocessor system having a variable speed system clock is disclosed herein. The microprocessor system includes an integrated circuit having a central processing unit and a ring oscillator variable speed system clock for clocking the microprocessor. The central processing unit and ring oscillator variable speed system clock each include a plurality of electronic devices of like type, which allows the central processing unit to operate at a variable processing frequency dependent upon a variable speed of the ring oscillator variable speed system clock. The microprocessor system may also include an input/output interface connected to exchange coupling control signals, address and data with the central processing unit. The input/output interface is independently clocked by a second clock connected thereto.

**10 Claims, 19 Drawing Sheets**





US005784584A

**United States Patent [19]**

Moore et al.

[11] Patent Number: **5,784,584**  
 [45] Date of Patent: **Jul. 21, 1998**

[54] **HIGH PERFORMANCE MICROPROCESSOR USING INSTRUCTIONS THAT OPERATE WITHIN INSTRUCTION GROUPS**

5,127,091 6/1992 Bonfaro et al. .... 395/375

[75] Inventors: **Charles H. Moore, Woodside; Russell H. Fish, III, Mt. View, both of Calif.**

*Primary Examiner—David Y. Eng  
Attorney, Agent, or Firm—Cooley Godward LLP*

[73] Assignee: **Patriot Scientific Corporation, San Diego, Calif.**

**ABSTRACT**

[21] Appl. No.: **484,935**

A high-performance microprocessor system using instruction that access operands and instructions located relative to the current instruction group rather than located relative to the current instructions, as is the convention, is disclosed herein. The microprocessor system includes a central processing unit, memory, and a bus connecting the central processing unit and memory. An instruction fetching unit, connected to the bus, is provided for fetching instruction groups from the memory for use by the central processing unit and for storage within an instruction register. An instruction supplying unit operates to supply, in succession from the instruction register to the central processing unit, one or more instructions from each of the instruction groups. The system further includes an instruction decoder for configuring the instruction supplying unit to select, from the instruction register, operands associated with instructions from particular instruction groups.

[22] Filed: **Jun. 7, 1995**

**Related U.S. Application Data**

[62] Division of Ser. No. 389,334, Aug. 3, 1989, Pat. No. 5,440,749.

[51] Int. Cl.<sup>6</sup> ..... **G06F 9/30**

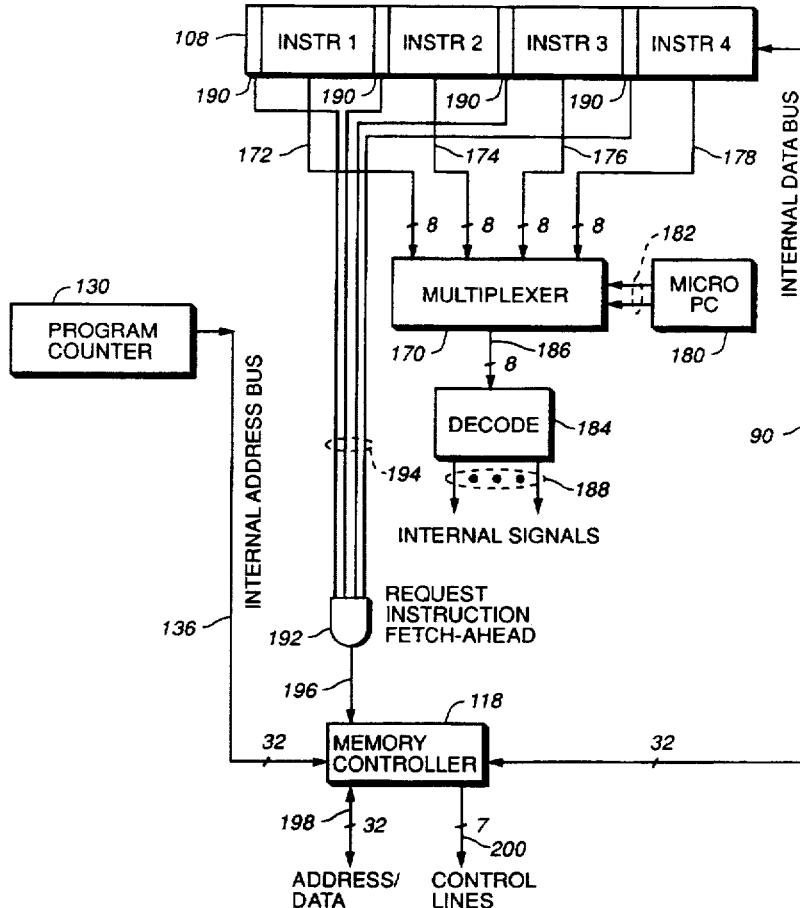
[52] U.S. Cl. .... **395/376**

[58] Field of Search ..... **395/376, 382, 395/384, 588, 800.23**

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4,967,326 10/1990 May ..... 395/800

**29 Claims, 19 Drawing Sheets**





US005440749A

**United States Patent [19]**

Moore et al.

[11] Patent Number: **5,440,749**  
 [45] Date of Patent: **Aug. 8, 1995**

**[54] HIGH PERFORMANCE, LOW COST MICROPROCESSOR ARCHITECTURE**

[75] Inventors: Charles H. Moore, Woodside; Russell H. Fish, III, Mt. View, both of Calif.

[73] Assignee: Nantronics Corporation, Eagle Point, Oreg.

[21] Appl. No.: 389,334

[22] Filed: **Aug. 3, 1989**

[51] Int. Cl.<sup>6</sup> ..... G06F 9/22

[52] U.S. Cl. ..... 395/800; 364/931; 364/925.6; 364/937.1; 364/965.4; 364/232.8; 364/244.3

[58] Field of Search ..... 395/425, 725, 775, 800

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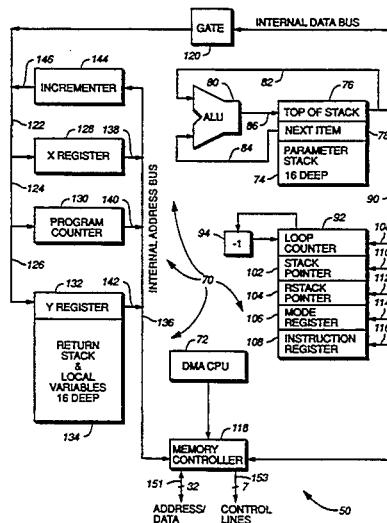
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*Primary Examiner*—David Y. Eng*Attorney, Agent, or Firm*—Cooley Godward Castro Huddleson & Tatum**[57] ABSTRACT**

A microprocessor (50) includes a main central processing unit (CPU) (70) and a separate direct memory access (DMA) CPU (72) in a single integrated circuit making up the microprocessor (50). The main CPU (70) has a first 16 deep push down stack (74), which has a to item register (76) and a next item register (78), respectively connected to provide inputs to an arithmetic logic unit (ALU) (80) by lines (82) and (84). An output of the ALU (80) is connected to the top item register at (82) is also connected by line (88) to an internal data bus (90). CPU (70) is pipeline free. The simplified CPU (70) requires fewer transistors to implement than pipelined architectures, yet produces performance which matches or exceeds existing techniques. The DMA CPU (72) provides inputs to the memory controller (118) on line (148). The memory controller (118) is connected to a RAM by address/data bus (150) and control lines (152). The DMA CPU (72) enables the CPU (70) to execute instructions four times faster than the RAM speed by fetching four instructions in a single memory cycle.

**29 Claims, 19 Drawing Sheets**



US006598148B1

(12) **United States Patent**  
**Moore et al.**

(10) **Patent No.:** US 6,598,148 B1  
(45) **Date of Patent:** Jul. 22, 2003

(54) **HIGH PERFORMANCE MICROPROCESSOR HAVING VARIABLE SPEED SYSTEM CLOCK**

(56)

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(75) Inventors: **Charles H. Moore**, Woodside, CA (US); **Russell H. Fish, III**, Dallas, TX (US)

(73) Assignee: **Patriot Scientific Corporation**, Poway, CA (US)

(\*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 09/124,623

(22) Filed: **Jul. 29, 1998**

(Under 37 CFR 1.47)

**Related U.S. Application Data**

(62) Division of application No. 08/484,918, filed on Jun. 7, 1995, now Pat. No. 5,809,336, which is a division of application No. 07/389,334, filed on Aug. 3, 1990, now Pat. No. 5,440,749.

(51) Int. Cl.<sup>7</sup> ..... **G06F 15/00**

(52) U.S. Cl. ..... **712/32**

(58) Field of Search ..... 712/32; 711/104, 711/105

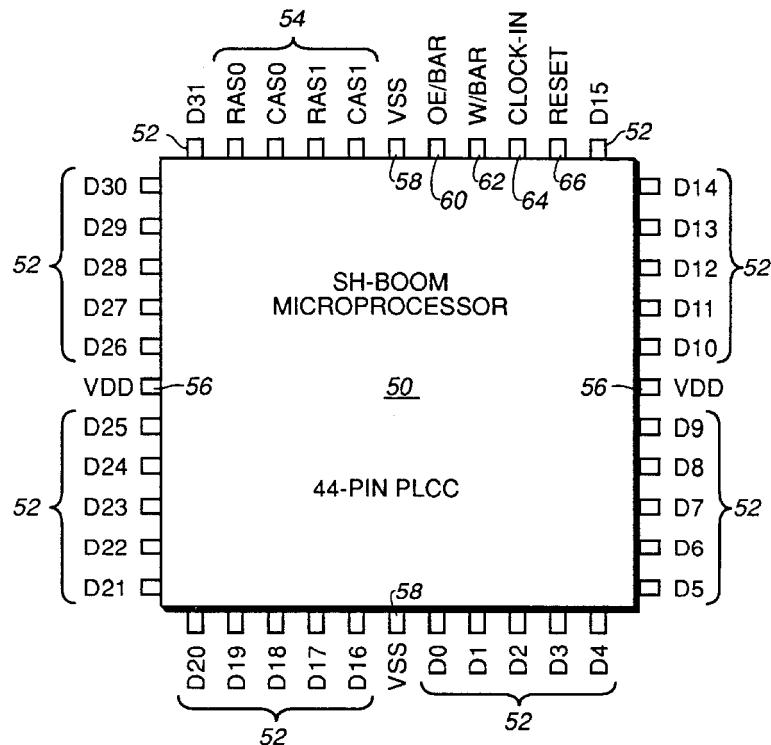
**Primary Examiner—David Y. Eng**

(74) Attorney, Agent, or Firm—Knobbe Martens Olson & Bear LLP

**ABSTRACT**

A microprocessor integrated circuit including a processing unit disposed upon an integrated circuit substrate is disclosed herein. The processing unit is designed to operate in accordance with a predefined sequence of program instructions stored within an instruction register. A memory, capable of storing information provided by the processing unit and occupying a larger area of the integrated circuit substrate than the processing unit, is also provided within the microprocessor integrated circuit. The memory may be implemented using, for example dynamic or static random-access memory. A variable output frequency system clock, such as generated by a ring oscillator, is also disposed on the integrated circuit substrate.

**13 Claims, 19 Drawing Sheets**





US005530890A

# United States Patent [19]

Moore et al.

[11] **Patent Number:** 5,530,890  
[45] **Date of Patent:** Jun. 25, 1996

- [54] **HIGH PERFORMANCE, LOW COST MICROPROCESSOR**

[75] Inventors: **Charles H. Moore**, Woodside; **Russell H. Fish, III**, Mt. View, both of Calif.

[73] Assignee: **Nantronics Corporation**, Eagle Point, Oreg.

[21] Appl. No.: **480,206**

[22] Filed: **Jun. 7, 1995**

#### **Related U.S. Application Data**

- [62] Division of Ser. No. 389,334, Aug. 3, 1989, Pat. No. 5,440,749.

[51] **Int. Cl.<sup>6</sup>** ..... **G06F 9/22**

[52] **U.S. Cl.** ..... **395/800**; 364/931; 364/925.6;  
364/937.1; 364/965.4; 364/232.8; 364/244.3

[58] **Field of Search** ..... 395/375, 500,  
395/775, 800

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4,354,228	10/1982	Moore et al. ....	395/800
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*Primary Examiner*—David Y. Eng  
*Attorney, Agent, or Firm*—Cooley Godward Castro Huddleston & Tatum

[57] ABSTRACT

A microprocessor (50) includes a main central processing unit (CPU) (70) and a separate direct memory access (DMA) CPU (72) in a single integrated circuit making up the microprocessor (50). The main CPU (70) has a first 16 deep push down stack (74), which has a top item register (76) and a next item register (78), respectively connected to provide inputs to an arithmetic logic unit (ALU) (80) by lines (82) and (84). An output of the ALU (80) is connected to the top item register (76) by line (86). The output of the top item register at (82) is also connected by line (88) to an internal data bus (90). A loop counter (92) is connected to a decrementer (94) by lines (96) and (98). The loop counter (92) is bidirectionally connected to the internal data bus (90) by line (100). Stack pointer (102), return stack pointer (104), mode register (106) and instruction register (108) are also connected to the internal data bus (90) by lines (110), (112), (114) and (116), respectively. The internal data bus (90) is connected to memory controller (118) and to gate (120). The gate (120) provides inputs on lines (122), (124), and (126) to X register (128), program counter (130) and Y register (132) of return push down stack (134). The X register (128), program counter (130) and Y register (132) provide outputs to internal address bus (136) on lines (138), (140) and (142). The internal address bus provides inputs to the memory controller (118) and to an incrementer (144). The incrementer (144) provides inputs to the X register, program counter and Y register via lines (146), (122), (124) and (126). The DMA CPU (72) provides inputs to the memory controller (118) on line (148). The memory controller (118) is connected to a RAM by address/data bus (150) and control lines (152).

## **10 Claims, 19 Drawing Sheets**

